CLAIMS:

1. A buffer circuit comprising:

a plurality of memory locations to hold data;

the memory locations of the plurality of memory locations addressable across an address space;

a read pointer to point a read address of the plurality of memory locations from which to read output data;

a write pointer to point a write address of the plurality of memory locations in which to write input data;

the read and the write pointers operable responsive to respective read and write clocks to sequence the read and write addresses across the address space of the plurality of memory locations;

a control register to define a nominal level; and

a controller to affect operation of the read pointer dependent on the write address of the write pointer, the read address of the read pointer, and the nominal level.

2. The circuit of claim 1, the controller operable to:

determine an amount of data in the buffer circuit based on a difference between the write address and the read address; and

enable the read pointer to increase the read address based on a difference between the amount of data determined and the nominal level.

3. The circuit of claim 2, in which the controller is further operable to at least hold the read address of the read pointer when the amount of data is determined to be less than the nominal level.

4. The circuit of claim 3, in which the control is further operable to decrement the read address when the amount of data is determined to be less than the nominal level.

5. The circuit of claim 3, in which the controller is further operable to advance the read address of the read pointer when the amount of data is determined to be greater than the nominal level.

6. The circuit of claim 5, in which the controller is further operable to disable the clock input to the read pointer and hold the read address upon determining the amount of data in the buffer circuit to be less than the nominal level.

7. The circuit of claim 5, in which the controller is operable to advance the read address by adjusting an increment to the read pointer responsive to determining the amount of data in the buffer circuit to be greater than the nominal level.

8. The circuit of claim 5, in which the controller is further operable to check if the amount of data determined differs from the nominal level by at least a threshold level before enabling the hold/advancement of the read address.

9. The circuit of claim 1, further comprising initialization circuitry to:

configure the write pointer with a predetermined start address for the write address; and

configure the read pointer with a beginning value based on the predetermined start address for the write address and the nominal level.

10. The circuit of claim 9, in which the beginning address for the read pointer is an address offset from the starting write address, and the offset is equal to the nominal level.

11. A channel alignment circuit comprising:

a plurality of buffers to buffer and synchronize data of multiple data channels;

a control register to receive a control value; and

correction logic to adjust data output from at least one buffer of the plurality of buffers dependent on an amount of data in the at least one buffer and the control value.

12. The circuit of claim 11, further comprising:

a variable latency register as the control register to receive and present a nominal fill value; and

a comparator to determine a difference between the amount of data in the at least one buffer and the nominal fill value presented by the variable latency register;

the correction logic operable to

pad data for output responsive to the comparator determining the amount of data in the at least one buffer less than the nominal fill value; and

omit data for output from the at least one buffer responsive to the comparator determining the amount of data in the at least one buffer greater than the nominal fill value.

13. The circuit of claim 12, wherein the nominal fill value has a magnitude less than a capacity of the at least one buffer.

14. The circuit of claim 12, the correction logic to enable the padding/omission of data when the amount of data in the at least one buffer differs from the nominal fill value by a magnitude greater than a predetermined threshold.

15. The circuit of claim 12, further comprising:

an input pointer to point an address of the at least one buffer in which to write data;

an output pointer to point an address of the at least one buffer from which to read data; and

logic to determine the amount of data in the at least one buffer based on the addresses of the input pointer and the output pointer.

16. The circuit of claim 15, further comprising:

first increment logic to increase the address of the input pointer responsive to a transition event of an input clock;

second increment logic to increase the address of the output pointer responsive to a transition event of an output clock;

the correction logic to advance the output pointer to omit data and to hold/decrement the output pointer to pad data.

17. The circuit of claim 11, further comprising:

minimum and maximum control registers as the control register to receive respective minimum and maximum fill values;

a first comparator to determine a difference between the amount of data in the at least one buffer and the minimum fill value; and

a second comparator to determine a difference between the amount of data in the at least one buffer and the maximum fill value;

the correction logic operable to

pad data for output responsive to the first comparator determining the amount of data in the at least one buffer is less than the minimum fill value; and

omit data for output from the at least one buffer responsive to the second comparator determining the amount of data in the at least one buffer is greater than the maximum fill value.

18. The circuit of claim 17, further comprising a generator to generate the minimum and maximum fill values based on the nominal fill value.

19. The circuit of claim 17, further comprising a generator to select the minimum and maximum values from one of a plurality of registers;

the generator to define the selection based on the nominal fill value.

20. The circuit of claim 11, in which the control register comprises at least one of the group consisting of a read/write memory, a content addressable memory, a look-up table, a programmable fabric and an increment/decrement register.

21. The circuit of claim 11, in which the correction logic further adjusts data output from the plurality of buffers dependent on the amount of data in the at least one buffer and the control value.

22. A data handling device comprising:

an input port to receive input data packets, the input port comprising a multi-block width;

a plurality of synchronization buffers to receive data of the input port;

an output port to present output data, the output port comprising a multi-block width;

buffers of the plurality of synchronization buffers to receive data from respective blocks of the input port and to present data to their associated blocks of the output port;

each of the plurality of synchronization buffers to output the data in synchronous, ordered relationship relative to the other synchronization buffers;

control circuitry to operate at least one synchronization buffer of the plurality of synchronization buffers within a nominal fill level;

a latency register to present a latency value, the latency register operable over a range of different latency values; and

circuitry to define the nominal fill level dependent on the latency value presented by the latency register.

23. The device of claim 22, in which the control circuitry is operable to:

determine an amount of data in the at least one synchronization buffer; and

pad/omit data to be output from the at least one synchronization buffer when the amount of data determined differs from the nominal fill level.

24. The device of claim 23, in which the control circuitry is further operable to pad/omit data to be output from the plurality of synchronization buffers when the amount of data determined differs from the nominal fill level.

25. The device of claim 24, in which an equal amount of data is padded/omitted in each synchronization buffer of the plurality of synchronization buffers.

26. The device of claim 23, in which the control circuitry is operable to enable the padding/omission when the amount of data determined differs from the nominal fill level by at least a predetermined threshold.

27. The device of claim 23, in which the latency register comprises at least one of the group consisting a read/write memory, a content addressable memory, a look-up table, a programmable fabric and an increment/decrement register.

28. The device of claim 23, in which

the at least one synchronization buffer comprises:

a first pointer to point a write address in which to write data into the at least one synchronization buffer, and

a second pointer to point a read address from which to read data from the at least one synchronization buffer; and

the control circuitry is to determine the amount of data in the at least one synchronization buffer based on the difference between the write address and the read address.

29. The device of claim 28, further comprising:

initialization circuitry to:

initialize the first pointer with a beginning write address;

initialize the second pointer with a beginning read address;

define the beginning write address and the beginning read address with an offset therebetween; and

define the offset dependent on the nominal fill level.

30. The device of claim 29, in which the initialization circuitry subtracts the nominal fill level from the beginning write address to define the beginning read address.

31. A method comprising:

defining a nominal fill for a buffer;

determining an amount of data in the buffer;

comparing the amount of data determined to the nominal fill defined; and

conditioning data of the buffer to be output dependent on the comparing.

32. The method of claim 31, further comprising:

identifying a latency performance for the buffer; and

defining the nominal fill based on the latency performance identified.

33. The method of claim 31, further comprising:

defining a maximum fill value and a minimum fill value based on the nominal fill;

the comparing comprises determining if the amount of data in the buffer is either less than the minimum fill value or greater than the maximum fill value.

34. The method of claim 31, in which the conditioning comprises:

padding data to be output responsive to the comparison determining that the amount of data in the buffer is less than the minimum fill value; and

omitting data to be output responsive to the comparison determining that the amount of data in the buffer is greater than the maximum fill value.

35. The method of claim 34, further comprising:

identifying a predetermined sequence of the data received in the buffer; and

padding/omitting data coincident with the predetermined sequence identified.

36. The method of claim 31, further comprising:

programming a configuration register with a value for the nominal fill;

the defining the nominal fill comprises obtaining the value from the configuration register.

37. The method of claim 31, further comprising:

defining beginning read and write addresses for the buffer, the beginning read and write addresses defined with an offset therebetween; and

using the nominal fill as the basis for the offset.

38. The method of claim 31, further comprising:

determining a packet length for data to be processed by the buffer; and

defining the nominal fill based on the packet length determined.

39. The method of claim 31, further comprising:

determining a frequency difference between a write clock for clocking data into the buffer and a read clock for clocking data out of the buffer;

the defining the nominal fill based on the frequency difference determined.

40. The method of claim 31, further comprising:

identifying a data transfer protocol, and

defining the nominal fill dependent on the protocol identified.

41. The method of claim 31, further comprising:

determining a maximum skew between corresponding data blocks of two different channels; and

defining the nominal fill dependent on the maximum skew determined.

42. The method of claim 31, further comprising receiving input data and determining a gap between packets of the input data;

the conditioning data of the buffer to comprise:

at least one of halting or decrementing the advancement of a write pointer to the buffer responsive to determining the gap in the input data received and

an amount of data in the buffer greater than the nominal fill; and

writing the input data received into locations of the buffer pointed by the write pointer.

43. The method of claim 42, in which the at least one of halting or decrementing in combination with the writing the input data received comprise over-writing locations of the buffer upon determining the gap in the input data and the amount of data in the buffer greater than the nominal fill.